Heavy Photon Search
Data Acquisition

Presented by
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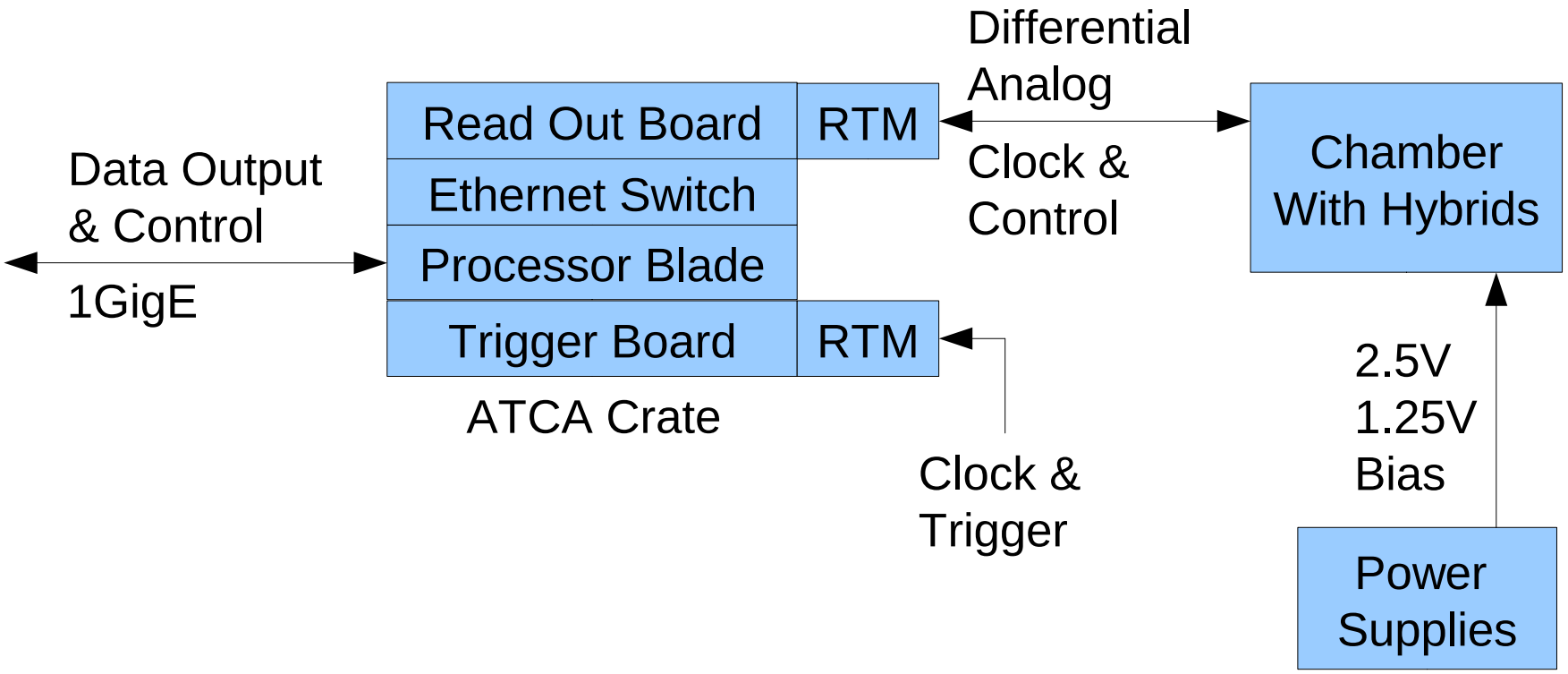
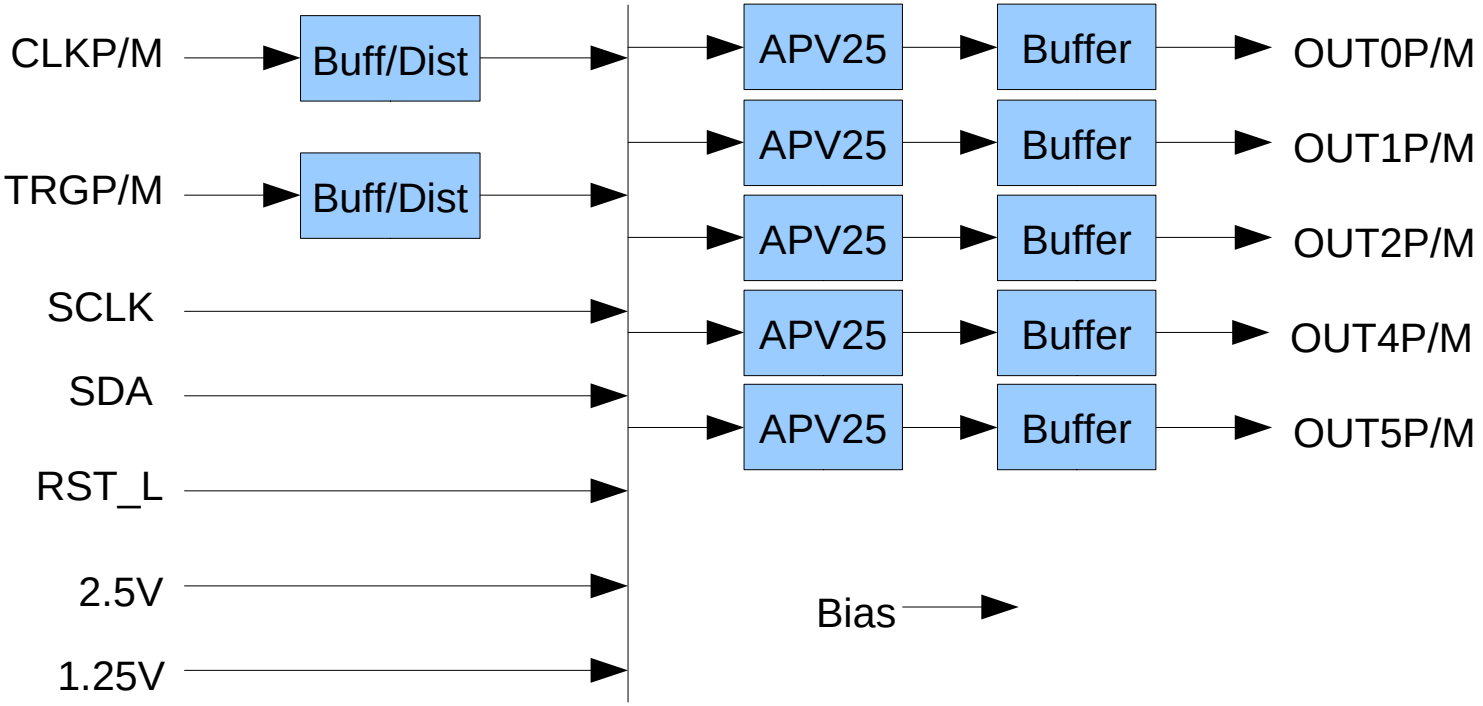
Overview



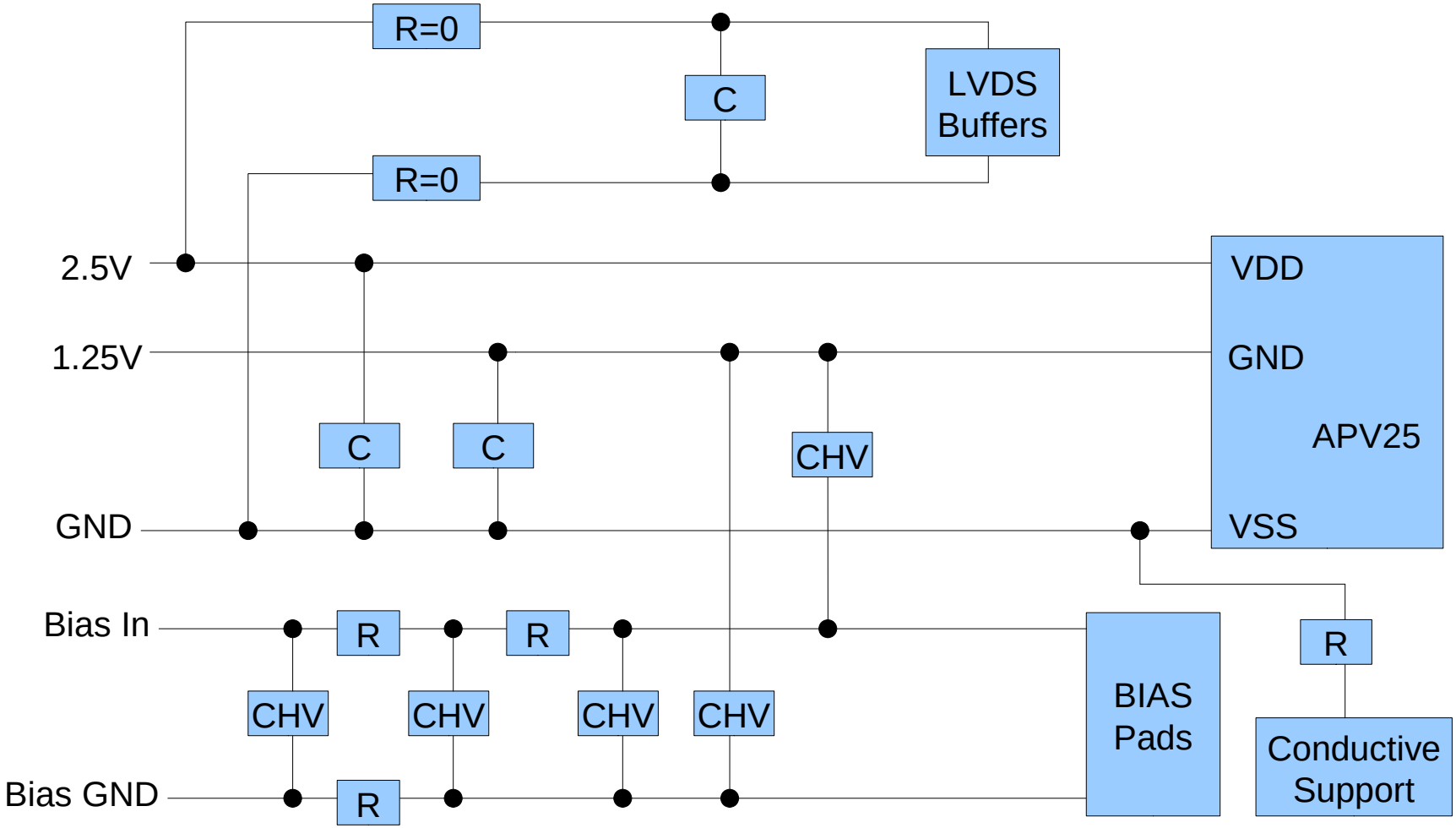
- **DAQ contained in ATCA chassis**
- **Common digital read out board**
  - **4 FPGA daughter boards each controlling 3 hybrids**
  - **Amplifier and ADC contained on RTM board**
- **Off-the-shelf ATCA processor blade supporting Linux OS**
- **Off-the-shelf ATCA switch card**
- **Trigger board for future integration**
  - **Same hardware as read out board with different RTM**

Hybrid



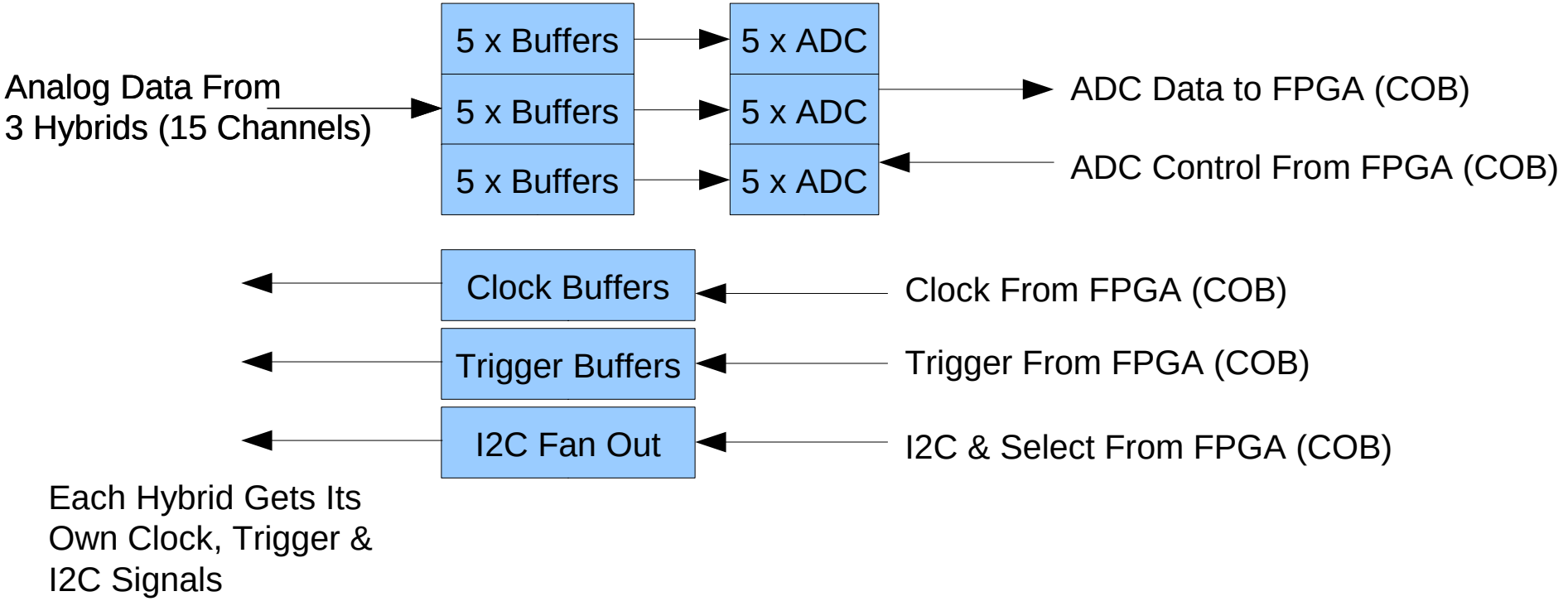
- **Incoming clock & trigger buffered, 2 loads per output (2.5V supply)**
- **Each APV25 has a unique I2C address**
  - **Each hybrid has its own I2C bus**
- **APV25 analog outputs buffered with gain = 1 differential amplifier**
  - **Gain is adjustable if required**
- **Power inputs distributed to all parts**
  - **2.5V = 690mA nominal / 1455mA worst case**
  - **1.25V = 325mA nominal / 825mA worst case**
  - **Bias routed directly to wire bond pads with local bypassing**
- **Internal APV25 current reference used**

Hybrid Power



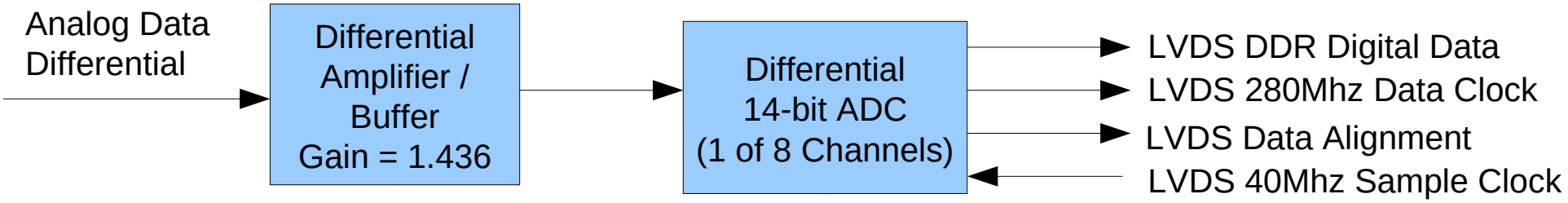
- **CHV capacitors are 2KV (Capacitor High Voltage)**
- **LVDS buffers isolated from APV25 planes/traces**
- **Conductive supports tied through impedance to GND**
  - **Output differential signals centered around 1.25V**
  - **ATCA chassis ground should be at same (or reasonably close) to GND on hybrid**
  - **Need to generate overall grounding diagram.**

RTM / COB Overview



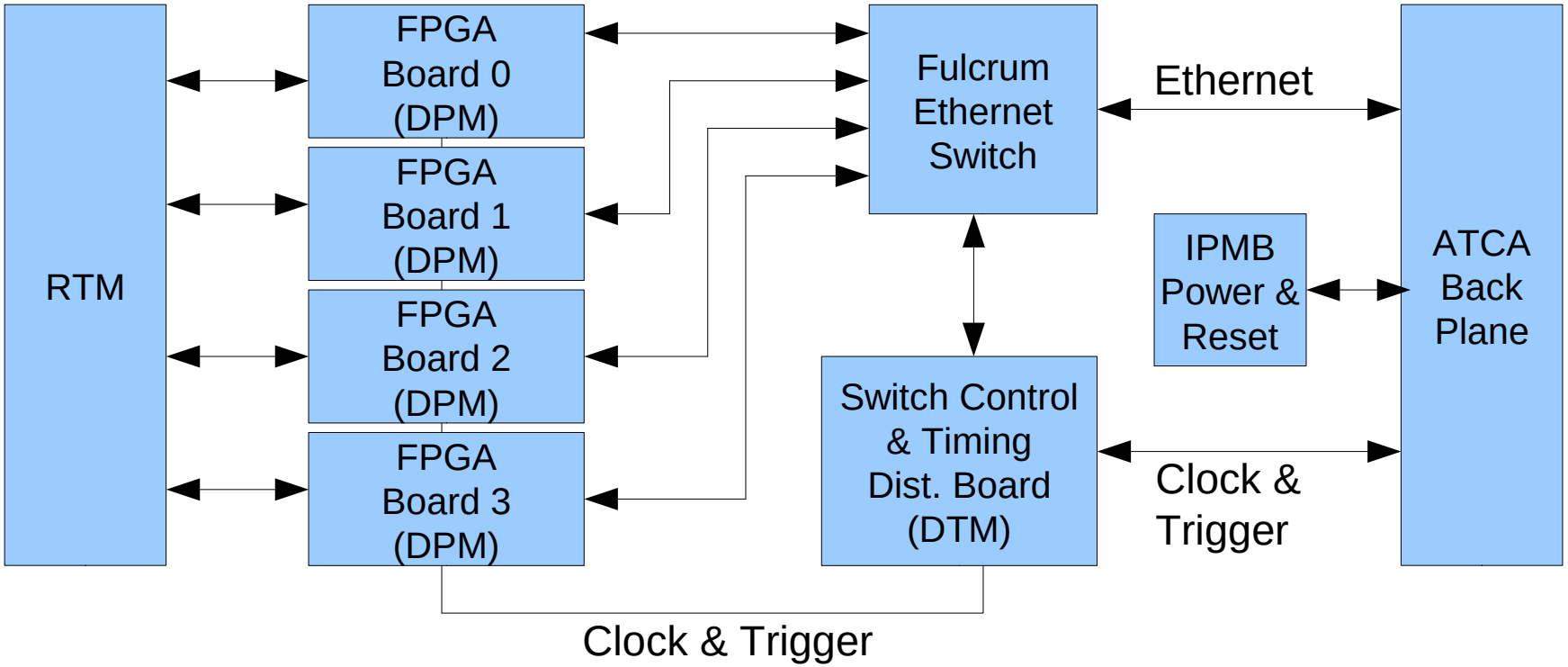
- **1 RTM per main board (COB – Carrier On Board)**
  - **COB supports 4 FPGA cards**
  - **Each COB FPGA connects To ¼ of an RTM**
- **¼ of an RTM supports 3 Hybrids (15 APV25s)**
  - **Total of 12 Hybrids (60 APV25s) per RTM/COB combination**
- **Independent clock & I2C per ¼ RTM**
- **2 8-Channel ADC devices per ¼ RTM, 8 ADCs in total**
- **I2C section uses transistor drivers & select lines, avoiding standard I2C buffers**

RTM



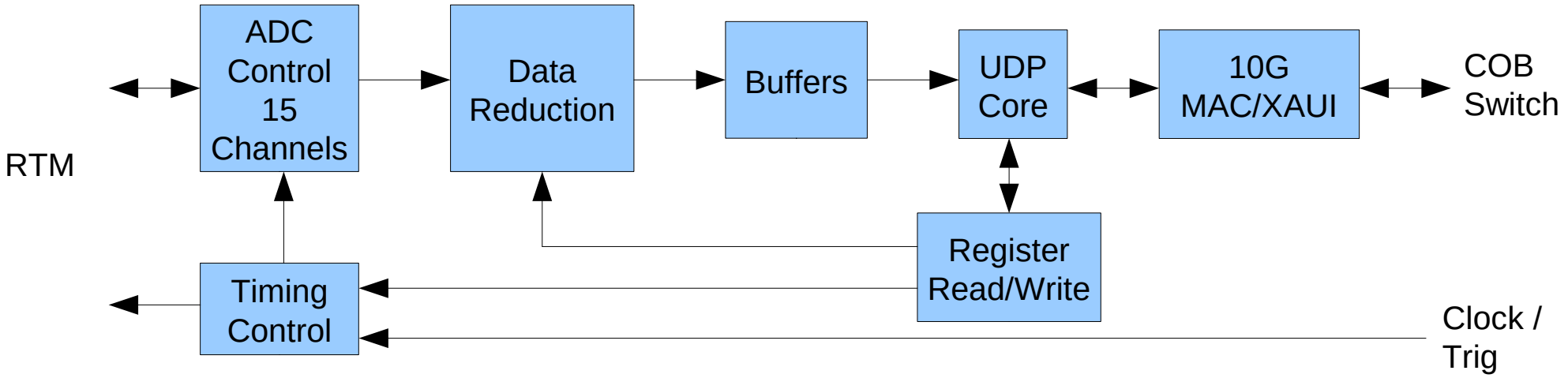
- **Input differential amplifier with Gain = 1.436 (replicated from ARC)**
  - **Input signal +/- 400mV * 1.436 = +/- 574mV**
  - **ADC range Is +/- 1V, room for increased gain**
  - **Add gain In Hybrid buffer?**
- **Input analog signal differentially terminated to 1.25V**
  - **Hybrid driver should have similar ground reference**
  - **Option to terminate with floating parallel resistor**
    - **Signal still needs to be close to 1.25V**
- **ADC continuously samples @ 40Mhz**
  - **FPGA chooses which samples are valid based upon trigger signal**
  - **14-bit differential ADC**
- **Separate clock from Hybrid distribution**
  - **Allows for sample phase adjustment**

COB Overview



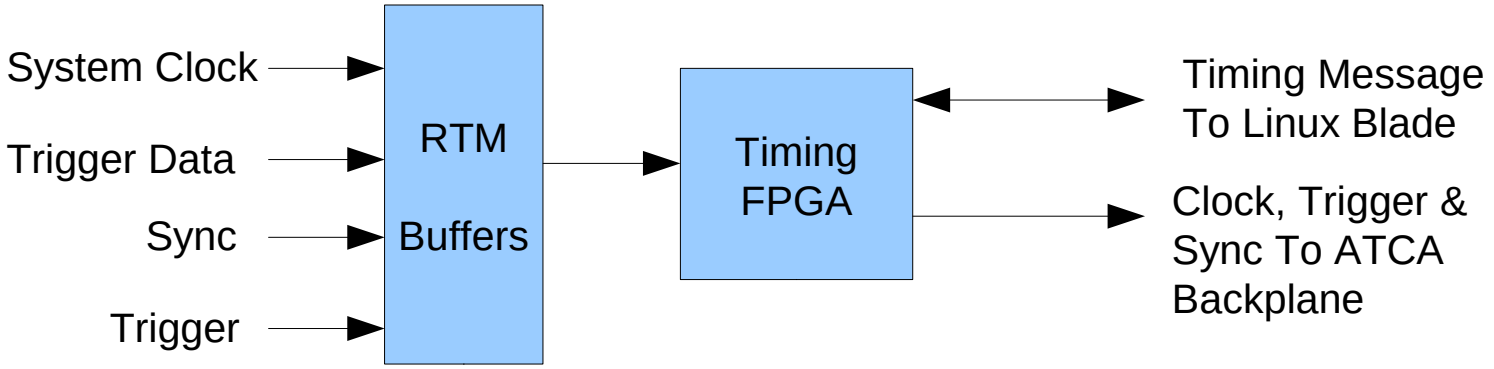
- **COB (Carrier On Board)**
  - **Developed at SLAC as standard DAQ platform**
  - **Supports 4 FPGA mezzanine cards (DPM)**
    - **Interconnected by Fulcrum Ethernet switch**
    - **Each has connection to ¼ RTM**
  - **Switch/Timing control board (DTM)**
    - **Simple clock fanout and EEPROM config of switch for our experiment**
    - **Supports more intelligent switch control & external IO for some applications**
    - **Fans out backplane timing & trigger signals to FPGA boards**

Data Processing FPGA (DPM)



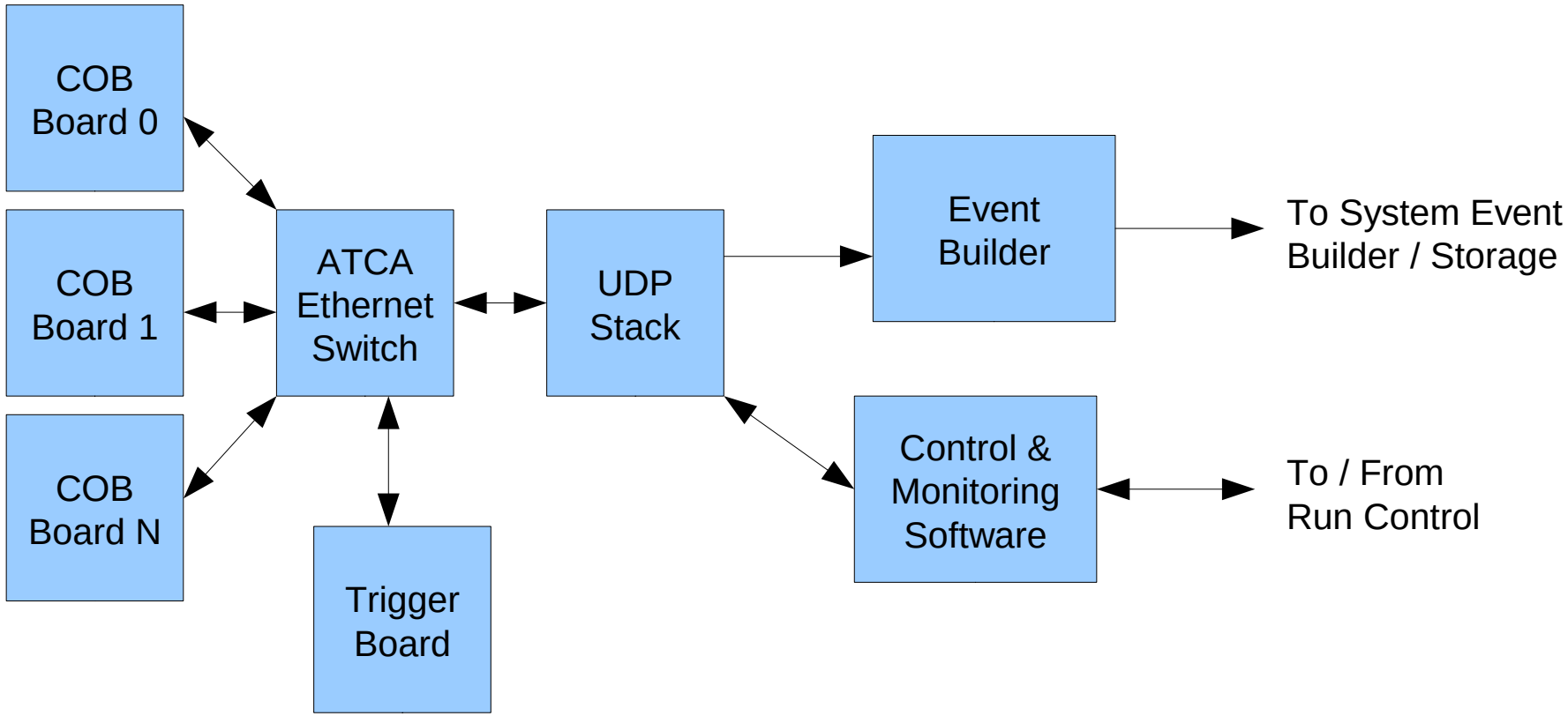
- **Incoming data stream**
  - **Trigger rate = 50Khz**
  - **Raw data rate = 15 APV25s * 128 Channels * 16-bits * 6 samples * 50Khz = 9.2Gbps**
  - **Assuming data rate of < 1Gbps after applying thresholds**
    - **Simple approach is to check if any of 6 samples are above threshold**
- **Each FPGA talks directly to ATCA Linux blade over UDP**
  - **Register read/write protocol**
  - **Bulk data transfer**
- **Trigger & clock distributed from back plane**
- **Optional buffering using DDR3 SDRAM module**
  - **Not needed but could be used to locally store some raw data to tune trigger**

Trigger Interface Board



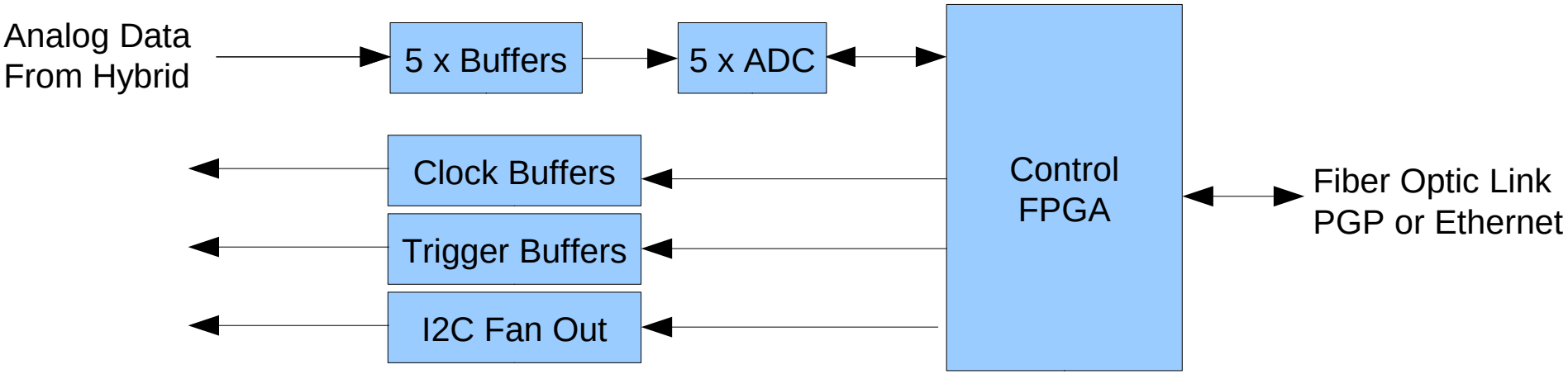
- **Standard ATCA clock & trigger distribution**
  - **Uses multi-drop LVDS backplane for clock & trigger**
- **Re-use of data processing board & FPGA**
- **Trigger board has only one FPGA daughter board (DPM) loaded**
- **Trigger specific RTM**
- **May be able to use front panel of DTM for timing signals on one of the readout boards**
  - **CTM is designed to support front panel IO**
  - **Eliminates extra ATCA blade**
  - **Any readout board can become timing master**

ATCA Processor Blade



- **Control & monitoring software**
  - **Manages & configures Hybrids & FPGAs**
  - **Collects and reports system/run status**
- **Event builder**
  - **Combines data from all FPGAs into a single event frame**
  - **Additional data reduction if necessary**

Development Board



- **Single board to support 1 Hybrid**
- **5 channels of input differential amplifier/buffer**
- **5 ADC channels (1 8-channel ADC chip)**
- **Small FPGA for data collection**
- **Fiber interface using SLAC standard DAQ protocol (PGP)**
  - **Existing generic software and control GUI for easy development**
  - **UDP can also be used**